REMARKS

Claims 1-11 remain in this application. Claims 1-11 have been amended. Support can be found on page 2, lines 7-9, page 4, lines 14-16, page 5, lines 7-15, page 6, lines 3-15, and page 7, lines 19-21. No new matter has been added.

Claims 1-11 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Negative voltage as used in claims 1-11 is the definition known and understood by someone skilled in the art, i.e., negative voltage (less than zero) with respect to the source voltage.

Claim 2 has been amended to delete the recitation to " and greater than zero"

Claims 1-6 and 7-11 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Terrill et al.

Terrill et al. is a SOI. Thus, there is an insulator layer 4, Fig. 1, on the Si substrate 6. Terrill et al. is a single semiconductor transistor. The Terrill et al. reference is trying to overcome a punchthrough problem due to short-channel effects, Col. 1, line 35-37. The prior art solution to the Terrill et al. problem was solved by increasing the dopant densities, Col. 1, lines 40-52. Terrill et al. solve the problem by providing a means for applying a back-gate bias voltage to induce both charge carriers in the channel region for MOSFET operation, and an electric field in the channel region for restricting punchthrough and other short-channel effects, claim 1.

The present invention is concerned with total dose radiation, an external radiation, and is not concerned with internal radiation due to the reduced size of the channel. The present invention as amended has a field oxide region separating each of the FETs on the substrate. It is not an SOI as there is no insulator 4 layer. In addition, the present invention is bulk CMOS or NMOS, thus, there is more than one transistor, i.e. two or more FETs. Each of the FETs is separated by a field oxide region which was neither suggested or taught in the Terrill et al. reference.

In the present invention, claims 1 and 7 have been amended to recite a bulk CMOS or NMOS device having two or more FETs on the substrate and a field oxide region separating each FET.

Claims 1 and 7 have been rejected under 35 U.S.C. § 102(b) as being anticipated by

Oashi et al.

Oashi et al. also relates to a SOI. The present invention is a bulk CMOS or NMOS device without the insulator layer, buried oxide layer, as shown in Fig 6.

The Federal Circuit in Constant v. Advanced Micro-Devices Inc., 7 U.S.P.Q.2d 1057, 1064 (Fed. Cir. 1988) stated: "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."

Thus, Terrill et al. does not anticipate claims 1 and 7. There is no disclosure in Terrill et al. with regard to a bulk CMOS or NMOS and separating each of the two or more FETs with a field oxide region as recited in amended claims 1 and 7. Oashi et al. does not anticipate claims 1 and 7 as there is no disclosure of a bulk CMOS or NMOS.

As claims 2-6 depend from and contain all the limitations of claim 1, it is felt that claims 2-6 distinguish from the references in the same manner as amended claim 1. As claims 8-11 depend from and contain all the limitations of claim 7, it is felt that claims 8-11 distinguish from the references in the same manner as amended claim 7.

In view of the foregoing, it is submitted that this application is now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In the event that a fee is required, please, charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please, credit Deposit Account No. 50-0281.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

1. (Amended) A bulk CMOS or NMOS device having [one] two or more [n-channel] FETs and having a field oxide region separating each FET which are disposed on a substrate, the device being resistant to total dose radiation failures, the device further comprising a negative voltage source, for applying a steady negative back bias to said substrate to increase the threshold voltage in a NMOS field oxide region to mitigate leakage currents in said device, thereby mitigating total dose radiation effects, wherein said field oxide region separates each FET.

2. (Amended) The device of claim1, wherein said back bias is less than the breakdown voltage of drain-substrate and source-substrate junctions[, and greater than zero].

7. (Amended) A method for operating a bulk CMOS or NMOS device to resist total dose radiation effects, said CMOS or NMOS device having [one] two or more [n-channel] FETs with a field oxide region separating each FET disposed on a substrate, comprising the steps of:

selecting a maximum ionizing radiation dose for operation of said bulk CMOS or NMOS device; and

determining and applying a negative back bias to said substrate of NMOS components of said bulk CMOS or NMOS device, wherein said negative back bias is sufficient to essentially eliminate leakage currents due to total dose radiation in [a] said field oxide region of said CMOS or NMOS device, thereby providing hardness against said maximum ionizing radiation dose.